SEMICONDUCTORS & **PECM**

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Semiconductor manufacturing is increasingly defined by its invisible geometries….

…Such as the thermal microchannels routed beneath high-power devices, the internal flow paths inside gas-handling hardware, and the sub-millimeter features that regulate heat, pressure and chemical purity at scale.

1

PECM is ideal for **semiconductor gas and fluid delivery components** where internal surface quality, feature consistency, and defect avoidance are critical.

2

PECM supports components that demand tight geometric control, repeatable features, and non-contact material removal, such as for **wafer processing equipment** and **tooling.**

3

PECM's capabilities are adept for **semiconductor thermal infrastructure** that relies on internal channels, microfeatures, or thin-walled geometries to manage heat efficiently.

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At-a-Glance: **PECM & Semicon** Features

PECM delivers consistent, unique value for semiconductor applications.

Maintaining consistent channel geometry, ultra-smooth surfaces, and predictable flow behavior across tens of thousands of components requires a process that eliminates thermal distortion, taper, and geometry drift across production runs.

Voxel's **PECM** can act as a unique remedy for these major semiconductor manufacturing challenges.

PECM removes metal **atom-by-atom**, generating **uniform internal surfaces and channel architectures** in copper, stainless steel, titanium, and other alloys across the semiconductor supply chain with high scalability.

PECM enables:

- **Micron-level channel uniformity** without taper, burrs or HAZ
- **<.2µm Ra internal surface finishes** on stainless, copper and nickel alloys
- **Repeatable multi-channel arrays** for thermal plays and flow-regulating components
- **Minimal tool wear**, supporting consistency across production

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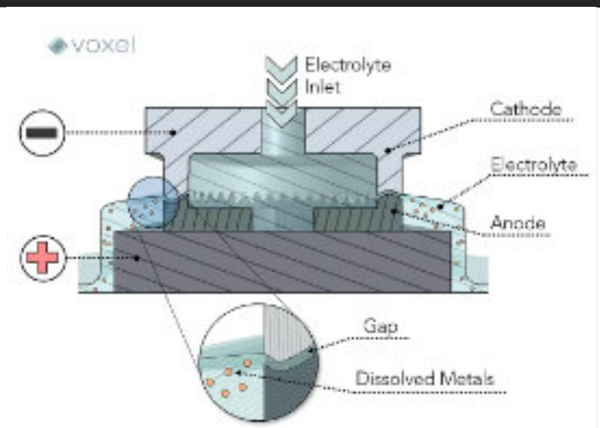
PECM **BASICS**



Unlike other material removal technologies such as electrical discharge machining (EDM), PECM is based on the principles of electrolysis. The machining operation involves a tool (the cathode) in the inverse shape of the desired workpiece (the anode).

As the tool moves towards the workpiece surface, it machines the workpiece into the complementary shape of the tool. This occurs as a pulsed DC current is applied, allowing for high precision and superior surface quality. At the same time, an electrolyte is pumped between the cathode and anode at high speed, removing dissolved metal and heat.

The result is an operation capable of producing a burr-free 3D shape with minimal tool wear in alloys that are difficult or impossible to machine through traditional methods. As PECM can produce parts in parallel with excellent repeatability, it is well-suited to high-volume and/or high-value production.

The PECM process has **4** factors:

- The **cathode**, or tool
- The **anode**, or workpiece
- The **electrolytic fluid,** and
- **The pulsed voltage**

Material **Compatibility**

PECM can most conductive materials, including but not limited to:

4140
A2 Tool Steel
Al MMCs
Aluminum 6061
Aluminum 7075
AMZ4
Brass
Bronze
CMSX-4
Cobalt Chrome
Copper
Ferrium C64
GaSb
Germanium
Haynes 230
Inconel 625
Inconel 718
Inconel 738
Inconel 740h
InSb
M4 Tool Steel
MarM247
Molybdenum
MP35N
NdFeB
Nickel
Nitinol
Nitronic 60
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Stainless 316
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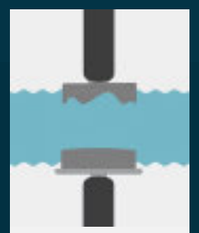
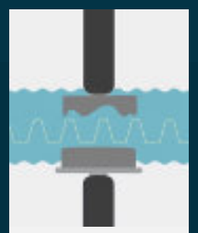
Ti Grade 2
Ti64
TiAl
Vit105



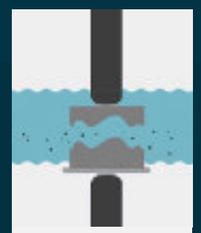
STEP 1

Cathode and anode are set up, and electrolyte is pumped between the two parts.



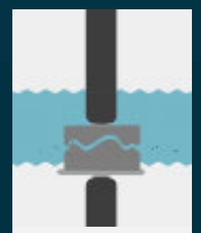
STEP 2

As the two pieces move together, a pulsed DC current is applied to the anode and cathode.



STEP 3

The flowing electrolyte removes heat and waste products from the gap.



STEP 4

The workpiece is machined into the complementary shape of the cathode tool.

STEP 5

Part is complete with no need for secondary process, burr removal or polishing.

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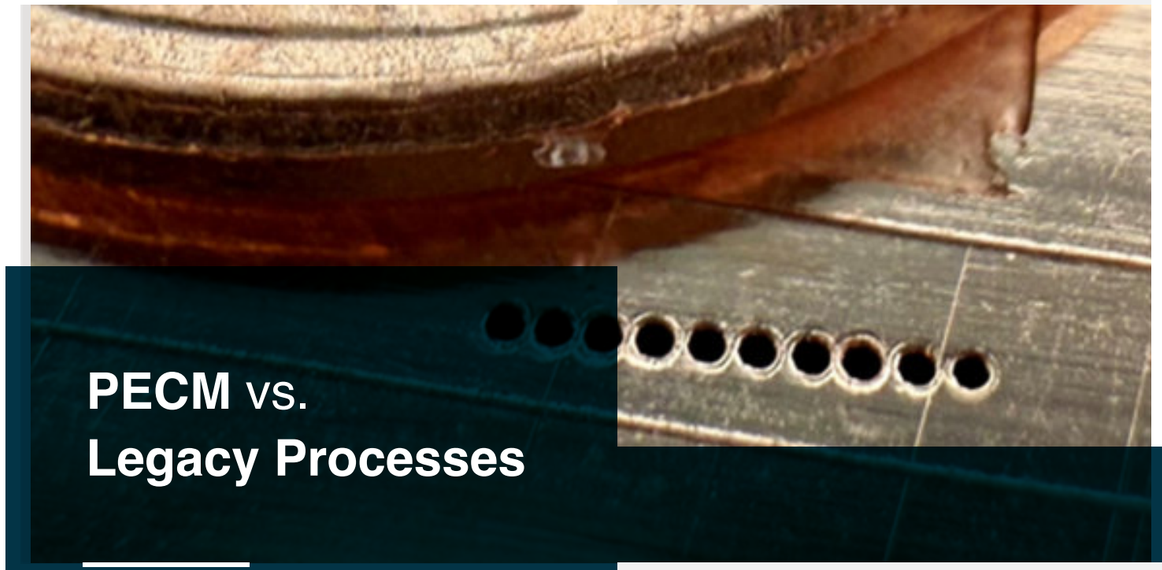

PECM vs. **Legacy Processes**

Design agency is limited by heat and/or contact-based material removal processes.

Conventional processes have inherent limitations, including…

Burrs & Tool Vibration

Contact-based machining introduces cutting forces that create **burrs, edge rollover,** and **vibration-driven surface damage**, notably on thin features and tight internal geometries.

Heat-affected Zones / Recast Layers

Thermal processes leave **HAZ, microcracks,** or **recast layers** that alter material properties, reducing fatigue or corrosion resistance.

Limited Repeatability

Repeatability degrades as tools wear and get replaced. **Dimensional drift, inconsistent finishes,** and **increased inspection** affect high-volume production.

Manufacturers are forced to compromise new designs to meet these limitations.

WHY CHOOSE PECM?

The unique properties of Voxel's pulsed electrochemical machining technology allow it to avoid many of the aforementioned issues:

- ☑ Non-contact machining produces **no burrs** or **tool vibration**, allowing machining of sensitive areas
- ☑ Non-thermal machining leaves **no HAZ** or **recast layers**, leaving **superfinished surfaces**
- ☑ PECM allows **part-to-part/ feature-to-feature repeatability**, significantly less tool wear

PECM IS FUNDAMENTALLY DIFFERENT

By utilizing electrochemistry instead of contact or heat, PECM removes material atom-by-atom, allowing smoother surface finishes, higher tolerances and improved repeatability– enabling manufacturers to explore new designs into production.

Process **Specs**

☑ Cut Surface Area

3500-7000mm2 in slower cuts; 1750-3500 in faster cuts. Larger surfaces may require multiple operations or higher-amperage equipment while smaller surfaces can potentially be run in-parallel

☑ Wall Thickness

Less than 50μm, with no maximum. .075mm (.003in) has been achieved in 2D blind or through features, minimum feature size is a wall of <25μm

☑ Slot Channel

•Top: 50μm (.002in) minimum
•Bottom: 20μm (.0008in) minimum
•Slot: 30 to 50μm
•Internal: 150μm (.006) minimum is most common, although 75μm (.003in) has been achieved in an ideal case

☑ Surface Finish

.005μm Ra to .4μm Ra, depending on the material

☑ Durability

Cathodes will have a lifetime exceeding thousands of parts

☑ Aspect Ratio

No minimum, capable of exceeding 300:1, depending on the feature size and electrode fabrication method

☑ Corners & Radii

•Top: 50μm (.002in) minimum; Bottom: 20μm (.0008in) minimum
•Minimum inside 90 corner radius, pocket bottom: 15-25μm possible; 25-50μm is more typical
•Minimum outside 90 corner radius, pocket top: 50μm standard
•Internal: 150μm (.006) minimum is most common, although 75μm (.003in) has been achieved in an ideal case

☑ Process Speed

Tends to be a step change in speed with geometry size, depending on the ability to flow electrolyte through the part's features.
Minimum blind feature (e.g. a slot): .5mm, speeds of .1-2μm/s
Feature of 2+mm: speeds of 15-30+ μm/s
More NRE yields more opportunity to improve speeds

☑ Depth Tolerance

Depends on parallelism of the workpiece. Generally, the depth can be controlled to +/- 5μm or less

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Industry **Outlook**

AI's rise has created near-explosive growth in semiconductor demand, especially for high-performance chips, causing a near-unprecedented wave of hyperscaling.

A November 2025 report from Google showed they must double their AI computing capacity every ~6 months to meet both internal and cloud customer demand **[1]**. Google's infrastructure VP revealed plans for a 1000x increase in AI capacity within 4-5 years. Data center space is at the epicenter of this record infrastructure investment: Microsoft has already installed enough data center infrastructure to continuously draw two nuclear-reactor-scale power plants' worth of electricity, 2GW worth.

However, this scalability is being severely limited. Both the Microsoft CEO and CFO have made public comments affirming that key issues withholding scalability are not necessarily from chip supply, but from **power, design, and cooling restraints.**

Problem 1: **Yield, Defectivity & Part Complexity**

Semiconductor manufacturing is deeply affected by the design, yield, and throughput issues encountered with **part miniaturization** for a few key reasons.

First, as transistors shrink, designs are increasingly sensitive to tiny flaws. Reports indicated Samsung's initial 3nm gate-all-around process suffered yields "around 10-50%" **[3]** compared to more mature processes yielding well above 90%. Even TSMC initially saw 3nm yields on the order of 60-70%, meaning many chips came out defective, and required an expensive wafer shakedown period to reach acceptable yields **[17]**.

Then, consider the increasing complexity of part designs, including FinFET, nanosheet transistors, deep trench contacts, etc, leading to further potential failures [18]. Shorts or opens are increasingly common

in critical circuits. For example, GlobalFoundries engineers recently found that a certain standard cell layout at 14nm had marginal spacing in a double-patterned contact layer, causing ~5% yield loss until an optical proximity correction fix was implemented **[20]**. Minuscule pattern tweaks or process variations, notably on multi-patterning, can lead to tremendous variations in yield, and achieving uniform, defect-free patterns across a wafer seems increasingly challenging.

A variety of other back-end packaging challenges are limiting scale. Consider how the solder bumps connecting chips to substrates are generally unreliable below 40μm, and how next-gen, high-density packages are requiring thousands of connections far tighter than those tolerances. Solutions exist, but advanced methods like direct metal bonding tend to be significantly slower and more process-sensitive than solder reflow. For instance, Cu-Cu bonds often require thermocompression bonding at ~300C for around 15-60 minutes, compared to a few seconds from a mass reflow oven.

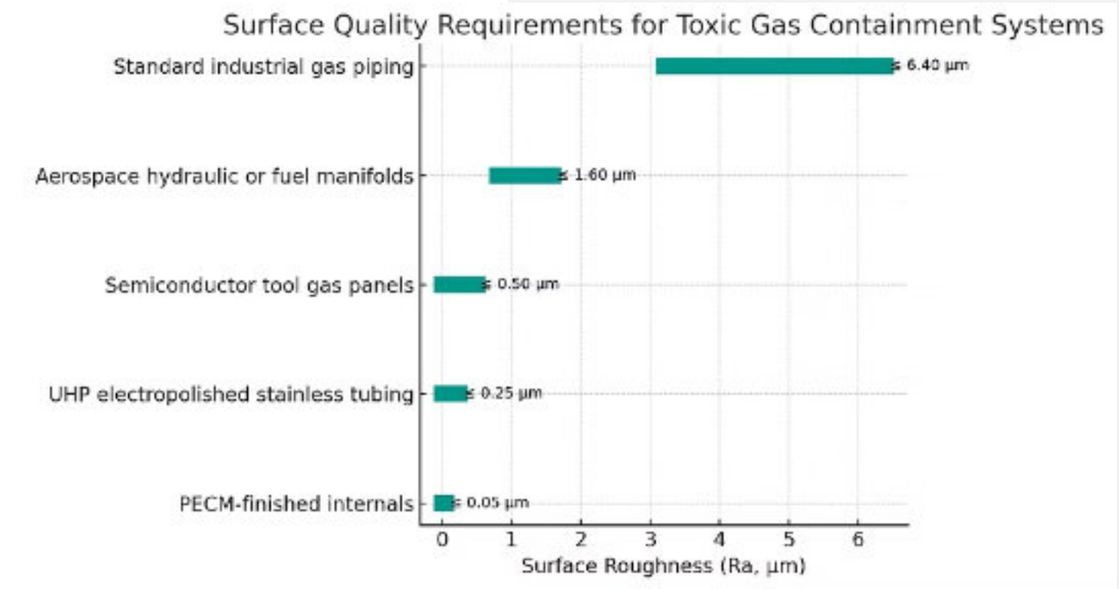
Problem 2: **Surfaces** & **Thermal Management**

Among the most important challenges facing the supporting infrastructure and equipment for semiconductor manufacturing, **surface quality,** has significant impact in two worlds:

- **UHP gas delivery systems** supplying process gases, and
- **Advanced cooling technologies** required to extract heat from chips

In the world of UHP infrastructure, minuscule issues in the form of microscopic surface imperfections, chemical residue, or contaminants can ruin both wafers and equipment–at times even leakage of 10^{-9}–10^{-11} std cm³/s (or a billionth of a cubic centimeter of gas per second) can be identified as problematic. This is equivalent to a grain of salt leaking every 8 hours.

Maintaining flawless gas delivery via ultra-smooth surfaces, leak-tight seals, and inert materials is an ongoing challenge for the industry due to both process limitations and the increasing sensitivity of process nodes.



Thermal infrastructure and advanced cooling techniques are an equally formidable challenge for semiconductor manufacturers, as the removal of heat from advanced chips (especially **direct-to-chip** cooling solutions) requires extremely advanced internal structures.

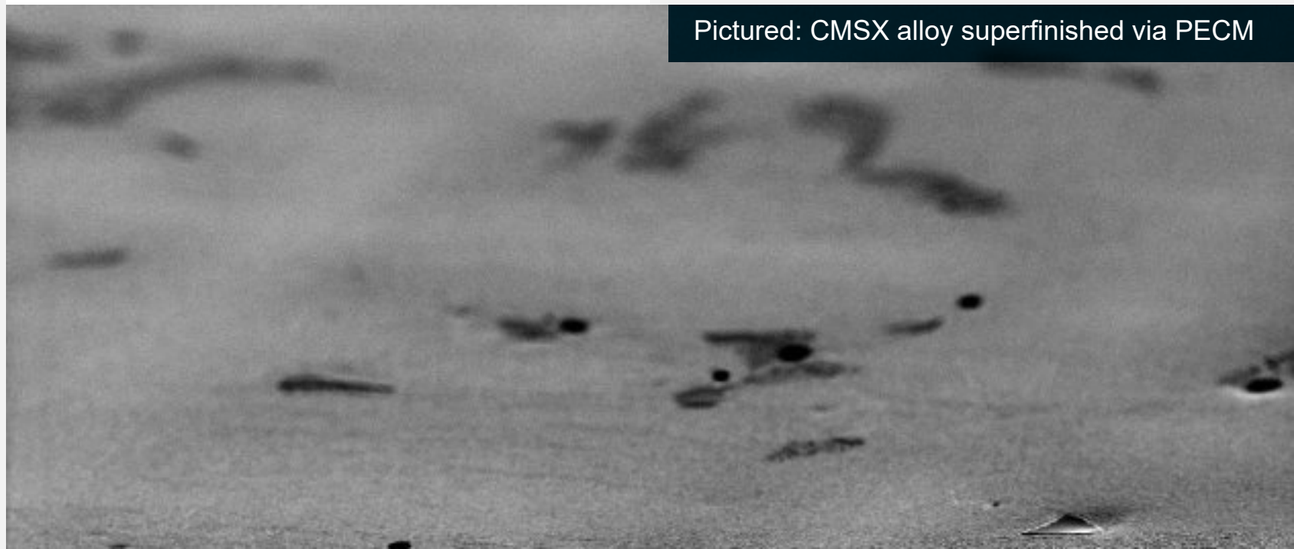
Consider how modern cold plates (liquid-cooled heat spreaders mounted on CPUs/GPUs) incorporate dense **microhole arrays** to increase surface area and heat transfer coefficient, each hole on the order of **tens of microns** in diameter. Leading-edge cooling designs from NVIDIA now feature microchannels down to 27μm. Not only are these tolerances critical, but their internal features directly affect the heat transfer ability of the component: roughness or particles can lead to clogs, hotspots, or particle contamination over time.

Micro-milling can produce these features, but with caveats– including burr formations and surface roughness challenges at micro-scale, especially as high-aspect ratio holes increase deflection risk and tool wear changing geometries hole-to-hole.

On the other hand, thermal-based processes, such as laser drilling and EDM, can scale much quicker– but can structurally alter the part in the form of **recast layers and heat affected zones (HAZ).** Postprocessing is often required, but post-etching can struggle to reach deeper holes and geometry loss can still occur.

Additive manufacturing can create complex manifolds and internal channels needed for thermal designs, but overwhelmingly struggles to produce adequate surface quality– as-build roughnesses amongst more advanced methods can still yield 10-20μm surfaces. Additionally, as AM scales to meet higher volumes, manufacturers may sacrifice laser scanning strategies, powder sizes, and layer thicknesses to make parts quicker with inferior tolerances.

As AI infrastructure continues to hyperscale, manufacturers will feel growing pains in the form of power, cooling, yield, and verification.



Pictured: CMSX alloy superfinished via PECM

What comes **Next?**

By and large, these limitations come from infrastructure: hyperscalers are projecting extreme growth curves (e.g., capacity doubling cadence and multi-year step changes), while simultaneously acknowledging power and cooling constraints as major obstacles.

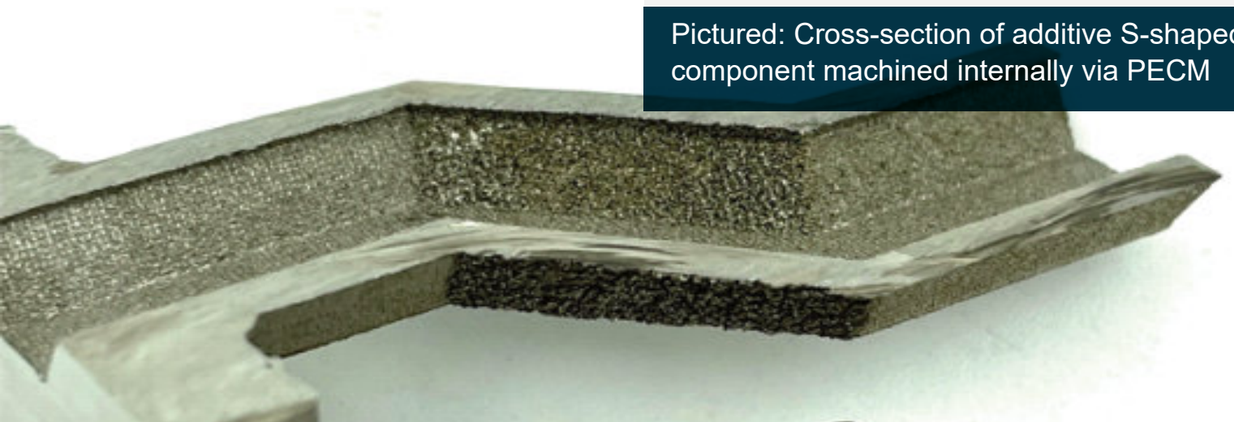
Geometry and **scale** are at the heart of these growing pains: when internal surfaces and microfeatures directly govern performance, manufacturers often respond by backing away from aggressive new geometries, as the risk of variability is increased at scale. This shows up as larger safety margins, lower feature densities, thicker walls, and more forgiving tolerances, ultimately resulting in a widening gap between what **can** be designed and what **does** get designed.

This "**design conservatism**" is especially true in thermal hardware where microchannels and dense arrays are pushing into tens of microns (e.g., 27 μm-scale features), and where a small amount of roughness or contamination can cause clogs, hotspots, or instability.

However, the market demands constant design innovation, and the conventional high-throughput processes manufacturers rely on to produce more complex-geometry components increasingly introduce structural side effects (e.g., recast layers / HAZ). While postprocessing can mitigate these issues, these methods struggle to uniformly reach deep microfeatures without altering geometry. Ultimately, that combination (tight microfeatures and hard-to-verify internal surfaces) increases the likelihood of throttling, drift, or shortened service life when systems are run continuously at high utilisation.

On the fab side, UHP distribution systems remain unforgiving: even extremely small leak rates and microscopic surface contamination are treated as problematic because they can affect both wafers and equipment. As process nodes become more sensitive, manufacturers will increasingly prioritize both predictability and contamination control, again reinforcing a tendency toward conservative specs unless manufacturing and verification confidence is unusually high.

That's why semiconductor manufacturers are increasingly seeking processes that can deliver internal microfeatures and surface integrity at scale.



Pictured: Cross-section of additive S-shaped component machined internally via PECM

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Working With **Voxel**

Voxel is a uniquely specialized contract manufacturer deploying critical parts in production environments via PECM with applied R&D.

☑ Driven by Co-Development

Voxel embeds with our customers throughout the product lifecycle, creating value through **IP, licensing,** and **production contracts.**

☑ Unique Capabilities

Our applied R&D enables machining of challenging **features, materials,** and **surface conditions** impractical or impossible with legacy processes.

☑ Production-Ready Success

Voxel's PECM-based processes are engineered for r**epeatability** and **parallelization**, supporting the transition from early development to reliable, high-volume production with minimal process rework.

Voxel is not organized around selling a process or executing to a fixed print, but to work **alongside** engineering teams as manufacturing constraints are discovered, challenged and rewritten via continued, applied R&D. We engage early-on when materials, internal features, or surface requirements are still fluid, creating unique **partnerships** from qualification to production and beyond.

At our core is Voxel's proprietary application of PECM: continuously advanced through applied R&D and feedback. By vertically integrating electrolyte chemistry, cathode design, tooling and process control, we enable unique **internal geometry machining, superfinished surfaces** and **material machining** methodology.

Partnership **Roadmap**

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Contact our **Team**

WHY VOXEL?

Voxel integrates our **PECM technology** with **unique process expertise** to enable **repeatable**, production-rate manufacturing of complex metal parts for critical industries.

WHY NOW?

Engaging with Voxel early creates **leverage**: our applied R&D and production teams can influence geometries, surfaces, and material strategies, ultimately enabling **higher-performance parts**, **smoother qualification** and a more **direct path to production**.

GET IN TOUCH WITH OUR ENGINEERS:

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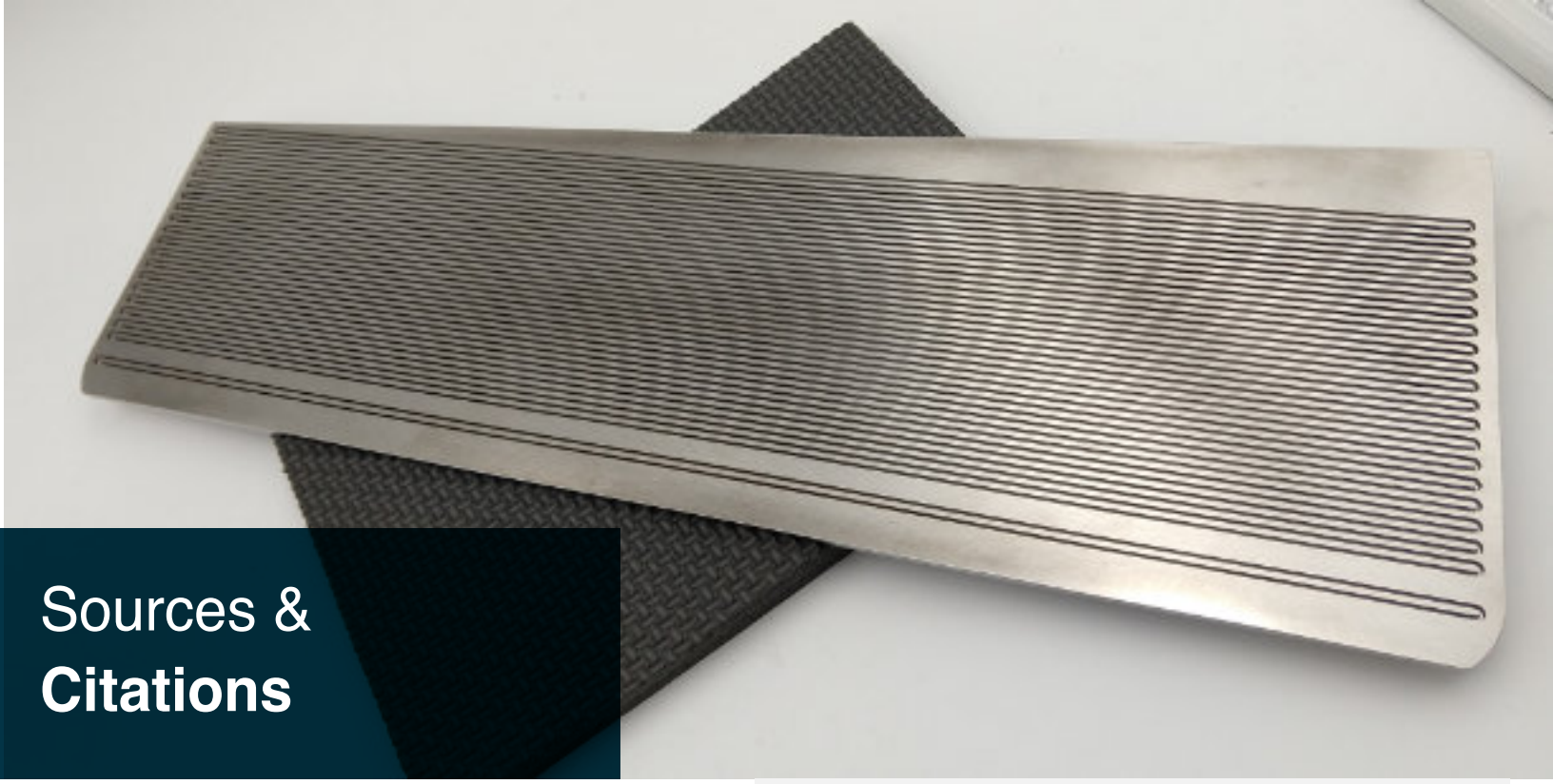

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